

## Gain and Attenuation Volume Controller IC 4 Sets of Stereo Input, Low voltage Gain and Attenuation 15~-79dB

### FEATURES

- Operation range: 2.7V~5.5V
- Low power consumption
- Gain/Attenuation: 15dB to -79dB at 1dB/step
- Good PSRR and low pop noise
- I<sup>2</sup>C interface
- Housed in 16 pin SOP, SSOP package

### APPLICATIONS

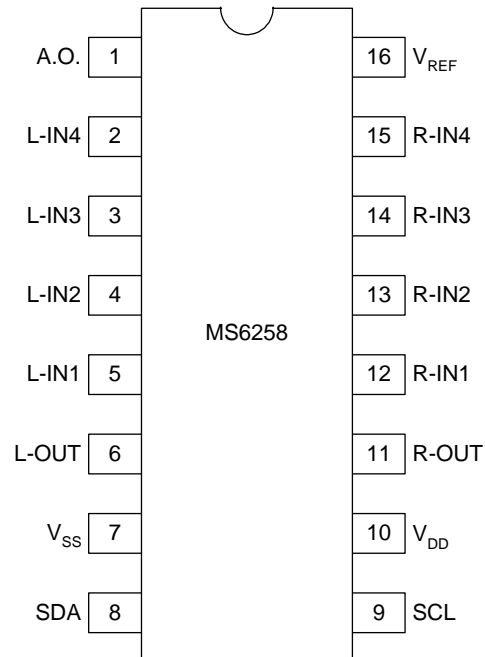
- Multimedia system
- Hi-Fi audio system
- MP3, PDA
- LCD Monitor

### DESCRIPTION

The MS6258 is a stereo audio volume controller IC with 4 sets of stereo input. It uses CMOS technology specially for the low voltage application with low noise, rail-to-rail output. The MS6258 provide an I<sup>2</sup>C control interface with gain / attenuation range of 15dB to -79dB, 1dB/step. The initial condition is set to be maximum attenuation -79dB and mute on mode when the power on.

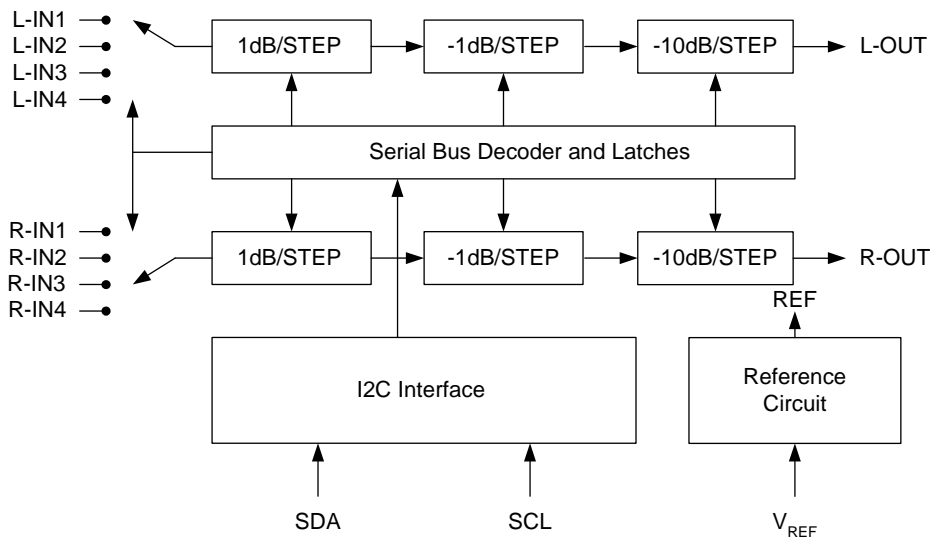
### PIN CONFIGURATION

| Symbol           | Pin | Description                            |
|------------------|-----|--|
| A.O.             | 1   | Address option *                       |
| L-IN4            | 2   | 4 <sup>th</sup> left channel input     |
| L-IN3            | 3   | 3 <sup>rd</sup> left channel input     |
| L-IN2            | 4   | 2 <sup>nd</sup> left channel input     |
| L-IN1            | 5   | 1 <sup>st</sup> left channel input     |
| L-OUT            | 6   | Left channel output                    |
| V <sub>SS</sub>  | 7   | Ground                                 |
| SDA              | 8   | I <sup>2</sup> C data input            |
| SCL              | 9   | I <sup>2</sup> C clock input           |
| V <sub>DD</sub>  | 10  | Positive supply voltage                |
| R-OUT            | 11  | Right channel output                   |
| R-IN1            | 12  | 1 <sup>st</sup> right channel input    |
| R-IN2            | 13  | 2 <sup>nd</sup> right channel input    |
| R-IN3            | 14  | 3 <sup>rd</sup> right channel input    |
| R-IN4            | 15  | 4 <sup>th</sup> right channel input    |
| V <sub>REF</sub> | 16  | Reference voltage = 1/2V <sub>DD</sub> |



- Note: 1. Pin 1 is set to Lo or open , the address code is 88H (10001000B).  
 2. Pin 1 is set to Hi , the address code is 8CH (10001100B).  
 3. The V<sub>REF</sub> connects a capacitor to V<sub>SS</sub>.

## BLOCK DIAGRAM



## ORDERING INFORMATION

| Package                 | Part number | Packaging Marking | Transport Media          |
|-------------------------|-------------|-------------------|--------------------------|
| 16-Pin SOP              | MS6258TR    | MS6258AS          | 2.5k Units Tape and Reel |
| 16-Pin SOP              | MS6258U     | MS6258AS          | 50 Units Tube            |
| 16-Pin SOP (lead free)  | MS6258GTR   | MS6258ASG         | 2.5k Units Tape and Reel |
| 16-Pin SOP (lead free)  | MS6258GU    | MS6258ASG         | 50 Units Tube            |
| 16-Pin SSOP             | MS6258SSTR  | MS6258            | 2.5k Units Tape and Reel |
| 16-Pin SSOP             | MS6258SSU   | MS6258            | 100 Units Tube           |
| 16-Pin SSOP (lead free) | MS6258SSGTR | MS6258G           | 2.5k Units Tape and Reel |
| 16-Pin SSOP (lead free) | MS6258SSGU  | MS6258G           | 100 Units Tube           |

## ABSOLUTE MAXIMUM RATINGS

| Symbol            | Parameter  | Rating        | Unit |
|-------------------|--|---------------|------|
| V <sub>DD</sub>   | Supply Voltage   | 6             | V    |
| V <sub>ESD</sub>  | Electrostatic Handling   | -4500 to 4500 | V    |
| T <sub>STG</sub>  | Storage Temperature Range  | -65 to 150    | °C   |
| T <sub>A</sub>    | Operating Ambient Temperature Range  | -40 to 85     | °C   |
| T <sub>J</sub>    | Maximum Junction Temperature   | 150           | °C   |
| T <sub>S</sub>    | Soldering Temperature, 10 seconds  | 260           | °C   |
| R <sub>THJA</sub> | Thermal Resistance from Junction to Ambient in Free Air<br>SOP16<br>SSOP16 | 210<br>210    | °C/W |

## OPERATING RATINGS

| Symbol          | Parameter      | Min | Typ | Max | Unit |
|-----------------|----------------|-----|-----|-----|------|
| V <sub>DD</sub> | Supply Voltage | 2.7 | -   | 5.5 | V    |

## 5V ELECTRICAL CHARACTERISTICS

( $V_{DD}=5.0V$ ,  $V_{SS}=0V$ , Attenuation=0dB, Gain=0dB,  $f=1kHz$ ,  $V_O=0dBV$ ,  $V_{REF}$  Cap=10uF; unless otherwise specified)

| Symbol                     | Parameter                            | Conditions              | Min         | Typ | Max         | Unit       |
|----------------------------|--------------------------------------|-------------------------|-------------|-----|-------------|------------|
| <b>DC Characteristics</b>  |                                      |                         |             |     |             |            |
| $I_Q$                      | Quiescent current                    |                         | -           | 3.8 | 4.2         | mA         |
| $A_{GA}$                   | Gain/Attenuation                     | Max gain                | -           | 15  | -           | dB         |
|                            |                                      | Max attenuation         | -           | -79 | -           | dB         |
| $A_{STEP}$                 | Gain/Attenuation step                |                         | -           | 1   | -           | dB         |
| $E_{GA}$                   | Gain/Attenuation step error          |                         | -           | 0.3 | -           | dB         |
| $E_{IGA}$                  | Interchannel gin/attenuation error   |                         | -           | 0.3 | -           | dB         |
| CS                         | Channel separation                   |                         | 95          | 105 | -           | dB         |
| PSRR                       | Power supply rejection ratio         | Vripple = -20dBV, 100Hz | -           | 53  | -           | dB         |
| MUTE                       | Mute Attenuation                     | Vin=0dBV                | -           | 85  | -           | dB         |
| Rin                        | Input Impedance                      |                         | 18          | 20  | -           | k $\Omega$ |
| Rout                       | Output Impedance                     |                         | -           | 50  | 100         | $\Omega$   |
| <b>AC Characteristics</b>  |                                      |                         |             |     |             |            |
| $V_o$                      | Maximum output voltage swing         | (THD+N)/S < 0.1%        | -           | 4.8 | -           | Vpp        |
| THD+N                      | Total harmonic distortion plus noise |                         | -           | -69 | -64         | dB         |
| S/N                        | Signal-to-noise ratio                | $V_O=4.5V_{pp}$         | 95          | 100 | -           | dB         |
| <b>Bus Characteristics</b> |                                      |                         |             |     |             |            |
| $V_{IH}$                   | Bus high input level                 |                         | -           | -   | $0.7V_{DD}$ | V          |
| $V_{IL}$                   | Bus low input level                  |                         | $0.3V_{DD}$ | -   | -           | V          |

## 3.3V ELECTRICAL CHARACTERISTICS

( $V_{DD}=3.3V$ ,  $V_{SS}=0V$ , Attenuation=0dB, Gain=0dB,  $f=1kHz$ ,  $V_O=-3dBV$ ,  $V_{REF}$  Cap=10uF; unless otherwise specified)

| Symbol                    | Parameter                            | Conditions              | Min | Typ | Max | Unit |
|---------------------------|--------------------------------------|-------------------------|-----|-----|-----|------|
| <b>DC Characteristics</b> |                                      |                         |     |     |     |      |
| $I_Q$                     | Quiescent current                    |                         | -   | 3.7 | 4.1 | mA   |
| CS                        | Channel separation                   |                         | 90  | 100 | -   | dB   |
| PSRR                      | Power supply rejection ratio         | Vripple = -20dBV, 100Hz | -   | 52  | -   | dB   |
| MUTE                      | Mute Attenuation                     | Vin=-3dBV               | -   | 80  | -   | dB   |
| <b>AC Characteristics</b> |                                      |                         |     |     |     |      |
| $V_o$                     | Maximum output voltage swing         | (THD+N)/S < 0.1%        | -   | 3   | -   | Vpp  |
| THD+N                     | Total harmonic distortion plus noise |                         | -   | -69 | -64 | dB   |
| S/N                       | Signal-to-noise ratio                |                         | 85  | 90  | -   | dB   |

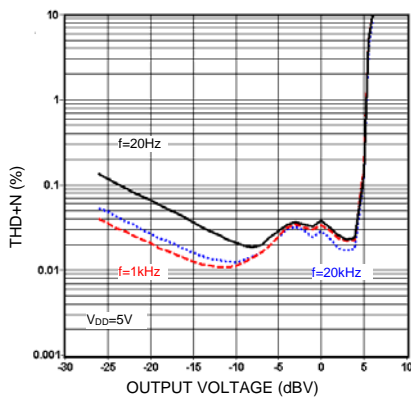
## 2.7V ELECTRICAL CHARACTERISTICS

( $V_{DD}=2.7V$ ,  $V_{SS}=0V$ , Attenuation=0dB, Gain=0dB,  $f=1kHz$ ,  $V_O=-3dBV$ ,  $V_{REF}$  Cap=10uF; unless otherwise specified)

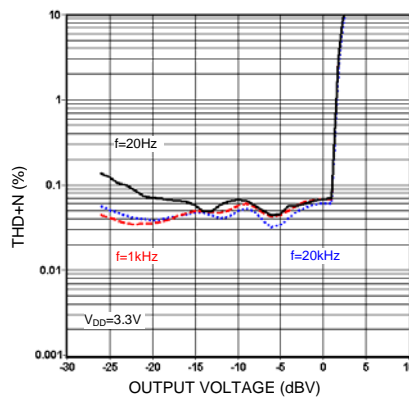
| Symbol                    | Parameter                            | Conditions                    | Min | Typ | Max | Unit            |
|---------------------------|--------------------------------------|-------------------------------|-----|-----|-----|-----------------|
| <b>DC Characteristics</b> |                                      |                               |     |     |     |                 |
| $I_Q$                     | Quiescent current                    |                               | -   | 3.2 | 3.6 | mA              |
| CS                        | Channel separation                   |                               | 90  | 100 | -   | dB              |
| PSRR                      | Power supply rejection ratio         | $V_{ripple} = -20dBV$ , 100Hz | -   | 50  | -   | dB              |
| MUTE                      | Mute Attenuation                     | $V_{in}=-3dBV$                | -   | 80  | -   | dB              |
| <b>AC Characteristics</b> |                                      |                               |     |     |     |                 |
| $V_o$                     | Maximum output voltage swing         | $(THD+N)/S < 0.3\%$           | -   | 2   | -   | V <sub>pp</sub> |
| THD+N                     | Total harmonic distortion plus noise |                               | -   | -69 | -64 | dB              |
| S/N                       | Signal-to-noise ratio                |                               | 85  | 90  | -   | dB              |

## TYPICAL PERFORMANCE CHARACTERISTICS

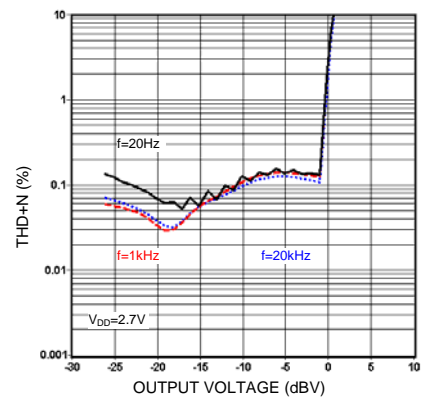
( $T_a=25^\circ C$ ,  $V_{REF}$  Cap=10uF; unless otherwise specified)



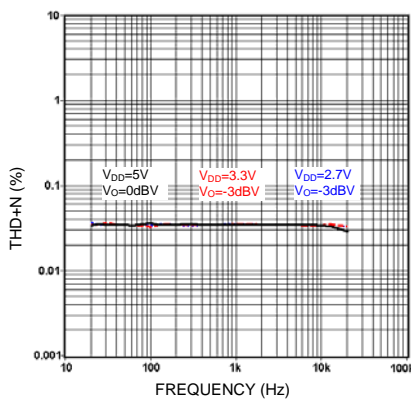
THD+N vs. output voltage



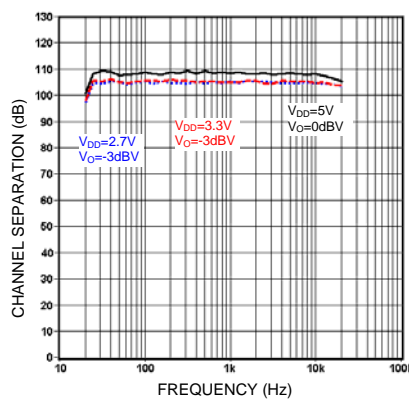
THD+N vs. output voltage



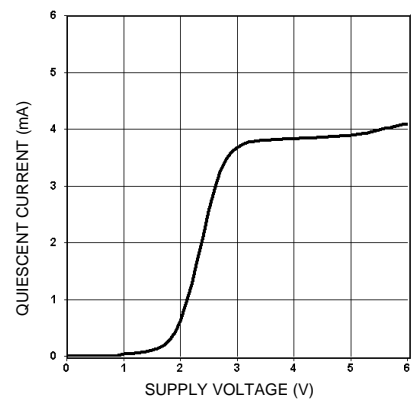
THD+N vs. output voltage



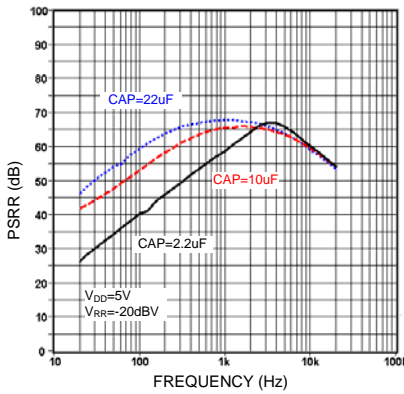
THD+N vs. frequency



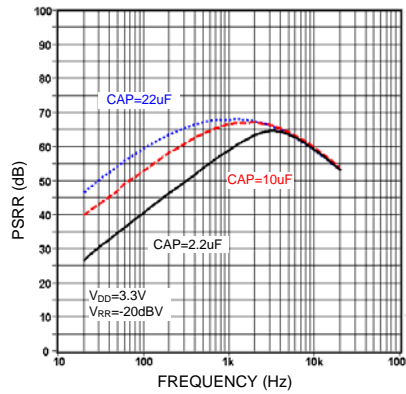
Channel separation vs. frequency



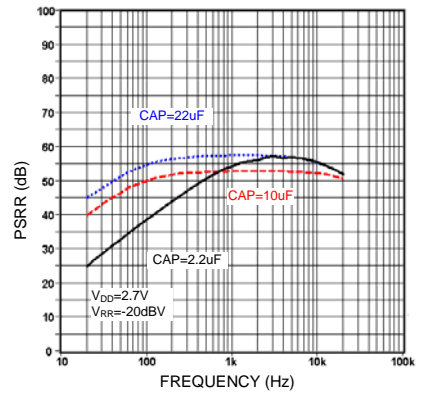
Quiescent current vs. supply voltage



PSRR vs. frequency



PSRR vs. frequency

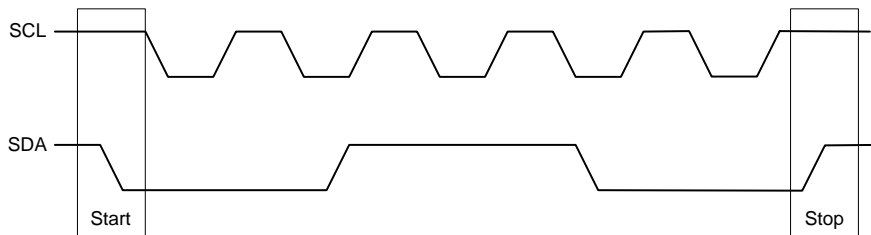


PSRR vs. frequency

## I<sup>2</sup>C BUS DESCRIPTION

### Start and stop conditions

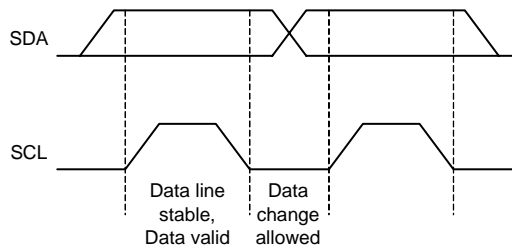
A start condition is activated when the SCL is set to HIGH and SDA shifts from HIGH to LOW state. The stop condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH state. Please refer to the timing diagram below.



SCL : Serial Clock Line, SDA : Serial Data Line

### Data validity

A data on the SDA line is considered valid and stable only when the SCL signal is in HIGH state. The HIGH and LOW states of the SDA line can only change when the SCL signal is LOW. Please refer to the figure below.

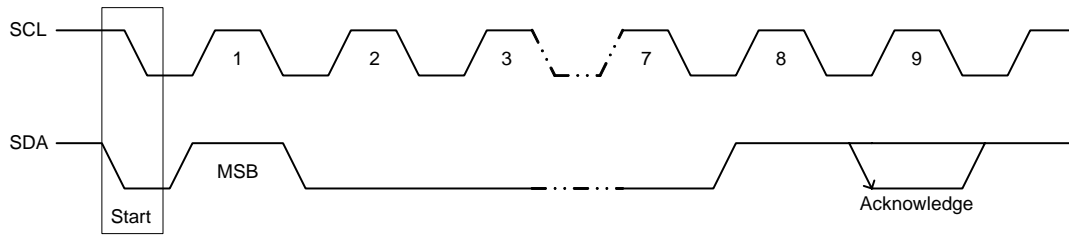


### Byte format

Every byte transmitted to the SDA line consists of 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transmitted first.

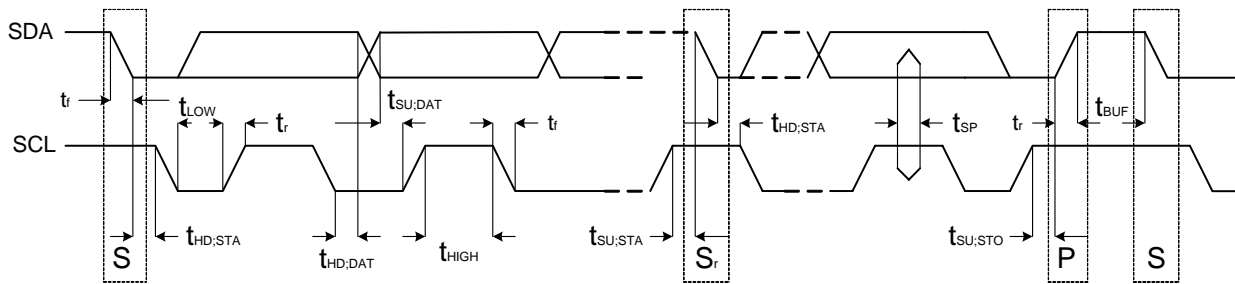
## Acknowledge

During the Acknowledge clock pulse, the master (up) put a resistive HIGH level on the SDA line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge clock pulse so that the SDA line is in a stable LOW state during this clock pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA line will remain at the HIGH level during the ninth (9<sup>th</sup>) clock pulse. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

## Timing of SDA and SCL bus lines

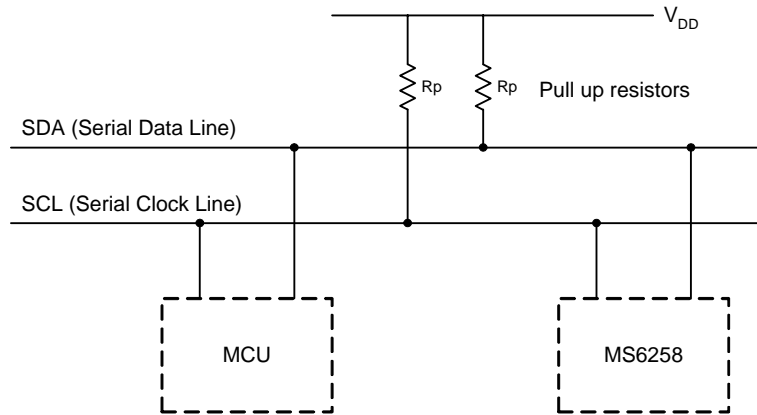


## Standard mode

| Symbol       | Parameter  | Min         | Max  | Unit |
|--------------|--|-------------|------|------|
| $f_{SCL}$    | SCL clock frequency  | 0           | 100  | kHz  |
| $t_{HD:STA}$ | Hold time (repeated) START condition.<br>After this period, the first clock pulse is generated | 4.0         | -    | us   |
| $t_{LOW}$    | LOW period of the SCL clock  | 4.7         | -    | us   |
| $t_{HIGH}$   | HIGH period of the SCL clock   | 4.0         | -    | us   |
| $t_{SU:STA}$ | Set-up time for a repeated START condition   | 4.7         | -    | us   |
| $t_{HD:DAT}$ | Data hold time:<br>For I <sup>2</sup> C-bus devices  | 0           | 3.45 | us   |
| $t_{SU:DAT}$ | Data-set-up time   | 250         | -    | ns   |
| $t_r$        | Rise time of both SDA and SCL signals  | -           | 1000 | ns   |
| $t_f$        | Fall time of both SDA and SCL signals  | -           | 300  | ns   |
| $t_{SU:STO}$ | Set-up time for STOP condition   | 4.0         | -    | us   |
| $t_{BUF}$    | Bus free time between a STOP and START condition   | 4.7         | -    | us   |
| $C_b$        | Capacitive load for each bus line  | -           | 400  | pF   |
| $V_{nL}$     | Noise margin at the LOW level for each connected device (including hysteresis)                 | $0.1V_{DD}$ | -    | V    |
| $V_{nH}$     | Noise margin at the HIGH level for each connected device (including hysteresis)                | $0.2V_{DD}$ | -    | V    |

## BUS INTERFACE

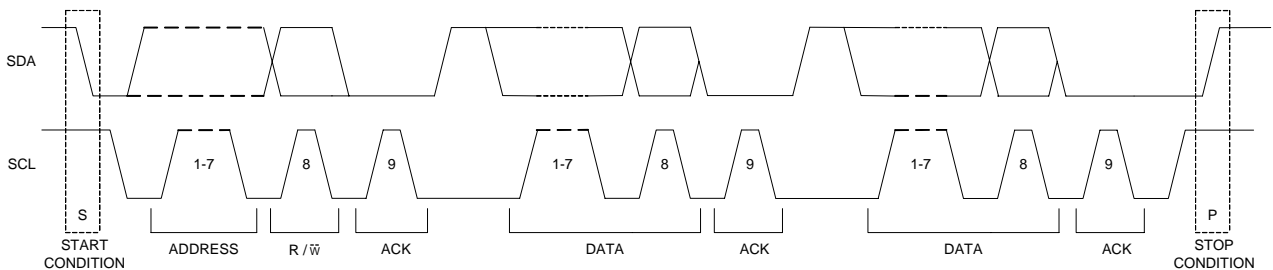
Data are transmitted to and from the MCU to the MS6258 via the SDA and SCL. The SDA and SCL make up the BUS interface. It should be noted that pull-up resistors must be connected to the positive supply voltage.



### Interface protocol

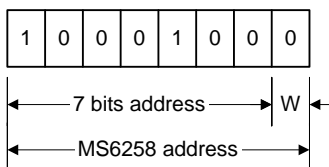
The format consists of the following

- A START condition
- A chip address byte including the MS6258 address. (7bits)
- The 8<sup>th</sup> bit of the byte must be "0".(write=0, read=1)
- MS6258 must always acknowledge the end of each transmitted byte.
- A data sequence (N-bytes + Acknowledge)
- A STOP condition

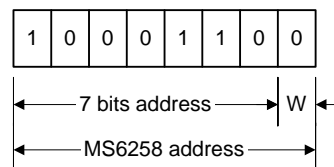


### Protocol Address

**Pin1(A.O.) = Low or Open**



**Pin1(A.O.) = High**



**Data bytes description**

| Function bits |   |   |   |    |    |    |     |  |
|---------------|---|---|---|----|----|----|-----|--|
| MSB           |   |   |   |    |    |    | LSB | Function                               |
| 1             | 1 | 1 | 1 | 1  | 1  | 1  | 1   | Function off (-79dB)                   |
| 1             | 1 | 0 | 1 | A3 | A2 | A1 | A0  | 2-channel, -1dB/step                   |
| 1             | 1 | 1 | 0 | 0  | B2 | B1 | B0  | 2-channel, -10dB/step                  |
| 1             | 0 | 1 | 0 | A3 | A2 | A1 | A0  | Left channel, -1dB/step                |
| 1             | 0 | 1 | 1 | 0  | B2 | B1 | B0  | Left channel, -10dB/step               |
| 0             | 0 | 1 | 0 | A3 | A2 | A1 | A0  | Right channel, -1dB/step               |
| 0             | 0 | 1 | 1 | 0  | B2 | B1 | B0  | Right channel, -10dB/step              |
| 1             | 1 | 0 | 0 | C3 | C2 | C1 | C0  | 2-channel, +1dB/step                   |
| 0             | 1 | 1 | 0 | C3 | C2 | C1 | C0  | Left channel, +1dB/step                |
| 0             | 1 | 0 | 1 | C3 | C2 | C1 | C0  | Right channel, +1dB/step               |
| 0             | 1 | 0 | 0 | 0  | 0  | 0  | 0   | Stereo1                                |
|               |   |   |   | 0  | 0  | 0  | 1   | Stereo2                                |
|               |   |   |   | 0  | 0  | 1  | 0   | Stereo3                                |
|               |   |   |   | 0  | 0  | 1  | 1   | Stereo4                                |
| 0             | 1 | 1 | 1 | 0  | 0  | 0  | 1   | Power off preparation (pop noise free) |
|               |   |   |   | 1  | 0  | 0  | 1   | 2-channel, mute On                     |
|               |   |   |   | 1  | 0  | 0  | 0   | 2-channel, mute Off                    |

| Gain / Attenuation bits |    |    |    |                               |     |     |
|-------------------------|----|----|----|-------------------------------|-----|-----|
| A3                      | A2 | A1 | A0 | Gain / Attenuation value (dB) |     |     |
| -                       | B2 | B1 | B0 | A                             | B   | C   |
| C3                      | C2 | C1 | C0 |                               |     |     |
| 0                       | 0  | 0  | 0  | 0                             | 0   | 0   |
| 0                       | 0  | 0  | 1  | -1                            | -10 | +1  |
| 0                       | 0  | 1  | 0  | -2                            | -20 | +2  |
| 0                       | 0  | 1  | 1  | -3                            | -30 | +3  |
| 0                       | 1  | 0  | 0  | -4                            | -40 | +4  |
| 0                       | 1  | 0  | 1  | -5                            | -50 | +5  |
| 0                       | 1  | 1  | 0  | -6                            | -60 | +6  |
| 0                       | 1  | 1  | 1  | -7                            | -70 | +7  |
| 1                       | 0  | 0  | 0  | -8                            | -   | +8  |
| 1                       | 0  | 0  | 1  | -9                            | -   | +9  |
| 1                       | 0  | 1  | 0  | -                             | -   | +10 |
| 1                       | 0  | 1  | 1  | -                             | -   | +11 |
| 1                       | 1  | 0  | 0  | -                             | -   | +12 |
| 1                       | 1  | 0  | 1  | -                             | -   | +13 |
| 1                       | 1  | 1  | 0  | -                             | -   | +14 |
| 1                       | 1  | 1  | 1  | -                             | -   | +15 |

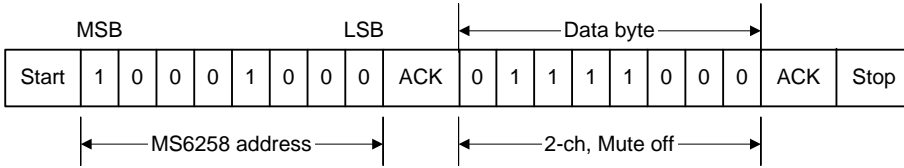
1. Where Ax=-1dB/step, Bx=-10dB/step, Cx=+1dB/step
2. The function of power off preparation is to prevent pop noise when power off.
3. The initial condition is set to be maximum attenuation -79dB and mute on mode when the power on.



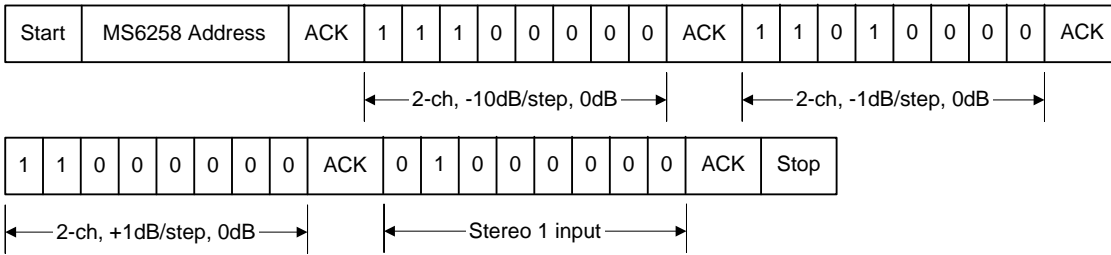
## Example

### Mute off

The initial condition is  $-79\text{dB}$  and mute on when power on. The first command must disable the mute function.

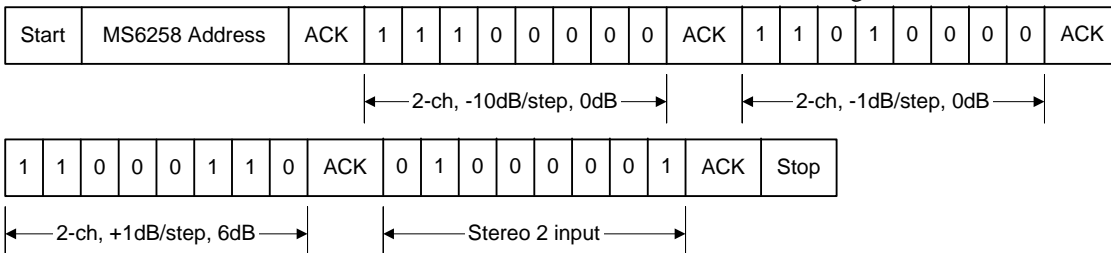


Set gain of 2 channel at  $0\text{dB}$ , and selected stereo 1 input.



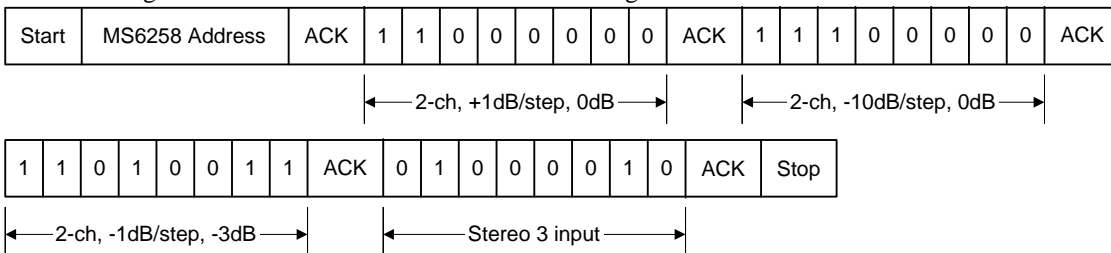
Set gain of 2 channel at  $6\text{dB}$ , and selected stereo 2 input.

The value of attenuation must be set zero when the volume from attenuation to gain.

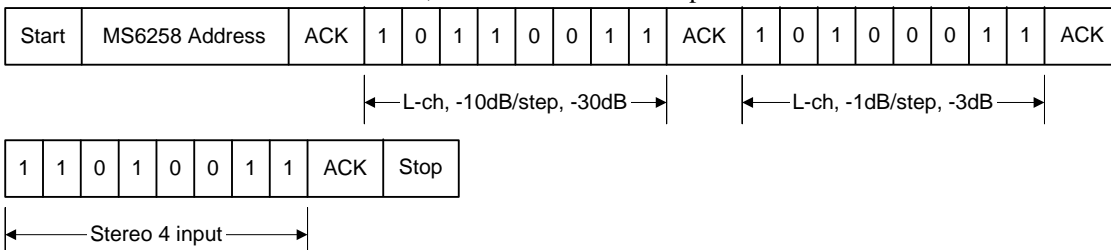


Set gain of 2 channel at  $-3\text{dB}$ , and selected stereo 3 input.

The value of gain must be set zero when the volume from gain to attenuation.

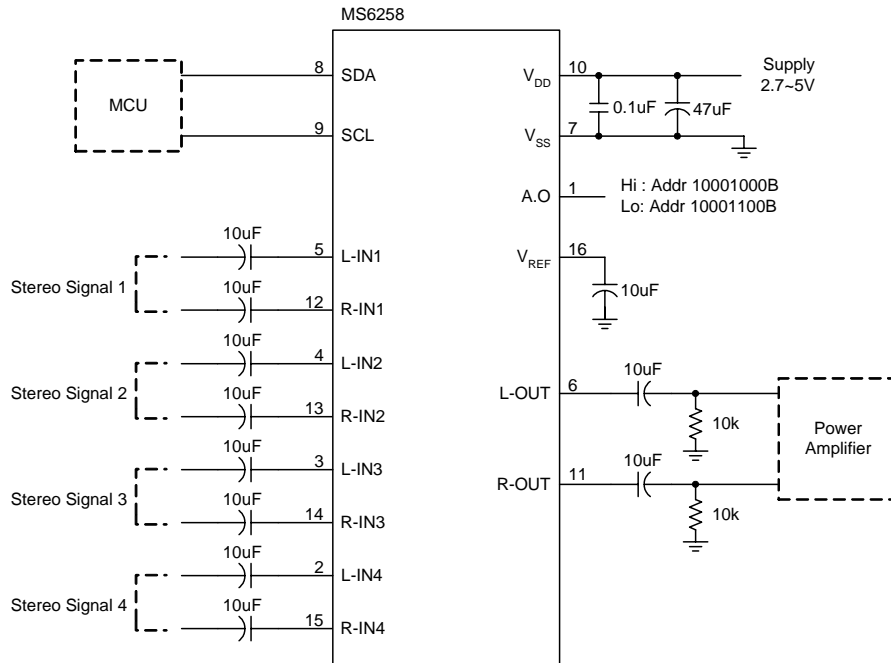


Set attenuation of left channel at  $-33\text{dB}$ , and selected stereo 3 input.

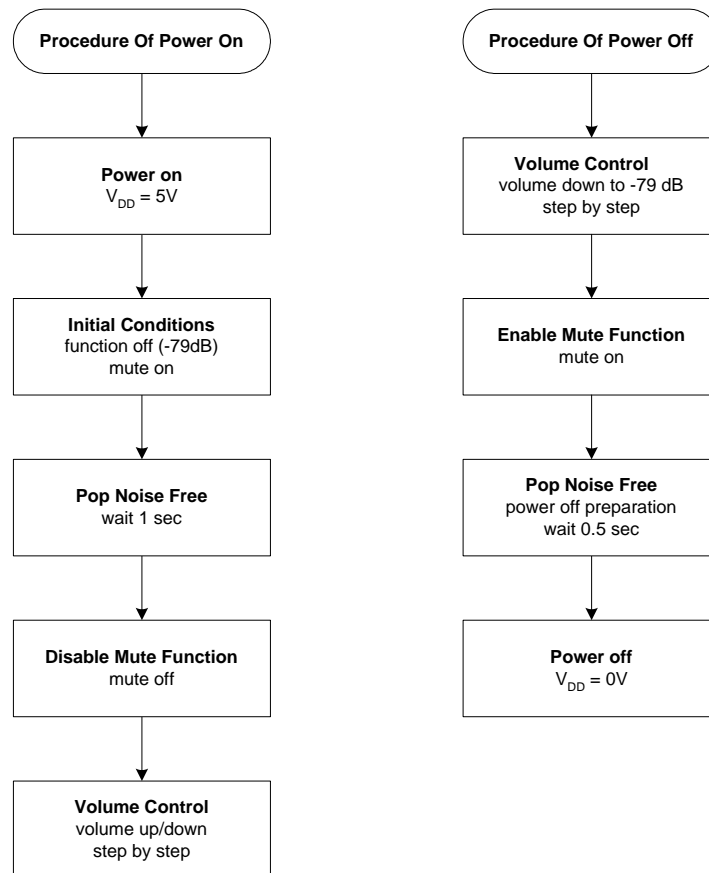


## APPLICATION INFORMATION

### Basic application example



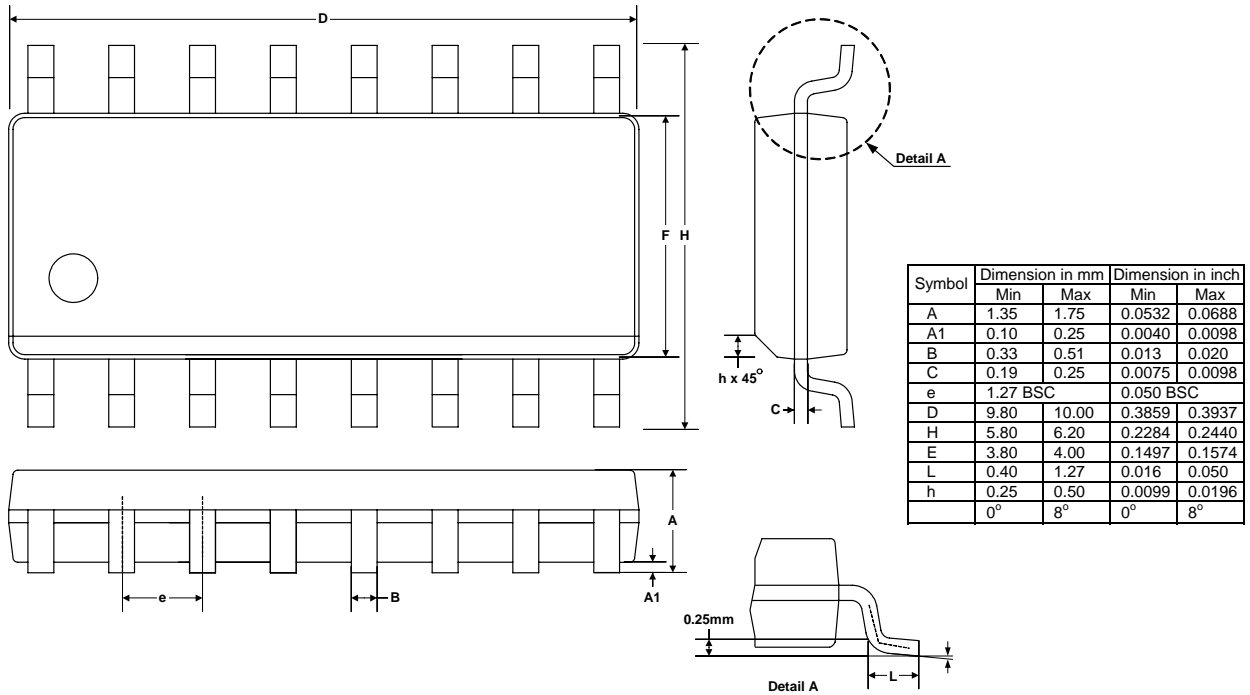
### Basic application flowchart



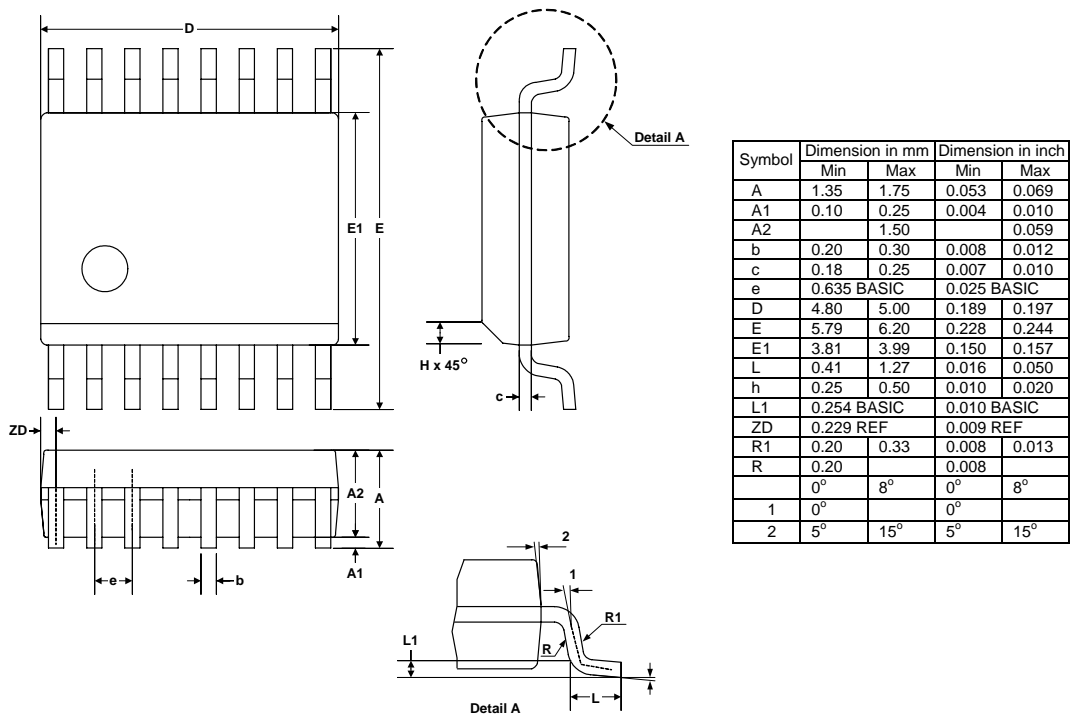
1. The initial condition is  $-79\text{dB}$  and mute on when power on.
2. In order to prevent pop noise when power on, please wait 1 sec to transmit I<sup>2</sup>C command.

## EXTERNAL DIMENSIONS

### SOP16

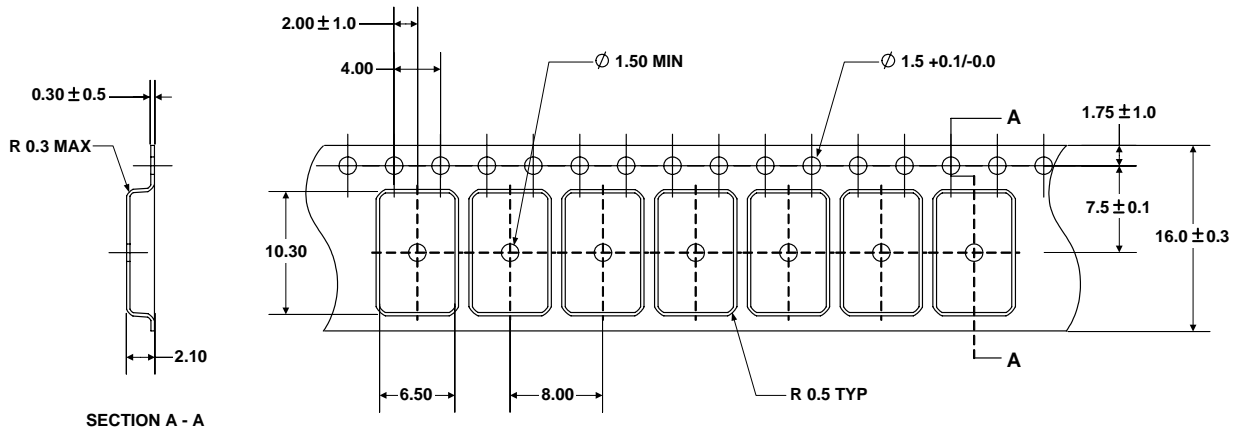


### SSOP16



**TAPE AND REEL (Unit : mm)**

**SOP16**



**SSOP16**

